CLAIMS

What is claimed is:

1. A method of testing a memory for faults, comprising:

writing a pattern of bits to a first memory block comprising a first plurality of bits of memory;

writing the pattern of bits to a second memory block comprising a second plurality of bits of memory;

reading the first plurality of bits of memory from the first memory block as a first plurality of read bits;

reading the second plurality of bits of memory from the second memory block as a second plurality of read bits; and

comparing each one of the first plurality of read bits with a corresponding one of the second plurality of read bits.

2. The method of claim 1, further comprising:

writing the pattern of bits to a third memory block comprising a third plurality of bits of memory;

reading the third plurality of bits of memory from the third memory block as a third plurality of read bits; and

comparing each one of the second plurality of read bits with a corresponding one of the third plurality of read bits.

3. The method of claim 2, further comprising comparing each one of the first plurality of read bits with a corresponding one of the third plurality of read bits.

4. The method of claim 2, further comprising determining that a fault has occurred in the second memory block when one of the second plurality of read bits differs from a corresponding one of the first plurality of read bits and differs from a corresponding one of the third plurality of read bits.

5. The method of claim 2, further comprising:

writing the pattern of bits to a fourth memory block comprising a fourth plurality of bits of memory;

reading the fourth plurality of bits of memory from the fourth memory block as a fourth plurality of read bits;

comparing each one of the third plurality of read bits with a corresponding one of the fourth plurality of read bits; and

comparing each one of the first plurality of read bits with a corresponding one of the fourth plurality of read bits.

6. The method of claim 5, further comprising determining that a fault has occurred in the second memory block when one of the second plurality of read bits differs from a corresponding one of the first plurality of read bits and differs from a corresponding one of the third plurality of read bits.

7. The method of claim 5, further comprising determining that a fault has occurred in at least two of a set of blocks of memory comprising the first memory block, the second memory block, the third memory block, and the fourth memory block when one of the first plurality of read bits differs from a corresponding one of the second plurality of read bits and a corresponding one of the third plurality of read bits differs from a corresponding one of the fourth plurality of read bits.

8. The method of claim 5, further comprising determining that a fault has occurred in at least two of a set of blocks of memory comprising the first memory block, the second memory block, the third memory block, and the fourth memory block when one of the first plurality of read bits differs from a corresponding one of the fourth plurality of read bits and a corresponding one of the third plurality of read bits differs from a corresponding one of the second plurality of read bits.

9. The method of claim 5, further comprising:

determining that a fault may have occurred in the second memory block when:

one of the first plurality of read bits differs from a corresponding one of the second plurality of read bits and a corresponding one of the third plurality of read bits differs from a corresponding one of the fourth plurality of read bits;

one of the first plurality of read bits differs from a corresponding one of the fourth plurality of read bits and a corresponding one of the third plurality of read bits differs from a corresponding one of the second plurality of read bits; or

one of the second plurality of read bits differs from a corresponding one of the first plurality of read bits and differs from a corresponding one of the third plurality of read bits.

10. The method of claim 1, further comprising generating the pattern of bits.

11. A method for dynamically testing and repairing a memory comprising:

testing a plurality of blocks of memory to identify a first faulty memory block;

identifying a spare memory block that has not been permanently remapped and that has not been temporarily remapped to replace a second faulty memory block; and

temporarily remapping the spare memory block to replace the first faulty memory block.

12. The method of claim 11, wherein the testing of the plurality of blocks of memory comprises:

writing a pattern of bits to a first memory block comprising a first plurality of bits of memory;

writing the pattern of bits to a second memory block comprising a second plurality of bits of memory;

reading the first plurality of bits of memory from the first memory block as a first plurality of read bits;

reading the second plurality of bits of memory from the second memory block as a second plurality of read bits; and

comparing each one of the first plurality of read bits with a corresponding one of the second plurality of read bits.

13. The method of claim 12, wherein the testing of the plurality of blocks of memory further comprises:

writing the pattern of bits to a third memory block comprising a third plurality of bits of memory;

reading the third plurality of bits of memory from the third memory block as a third plurality of read bits; and

comparing each one of the second plurality of read bits with a corresponding one of the third plurality of read bits.

14. The method of claim 13, wherein the testing of the plurality of blocks of memory further comprises:

writing the pattern of bits to a fourth memory block comprising a fourth plurality of bits of memory;

reading the fourth plurality of bits of memory from the fourth memory block as a fourth plurality of read bits;

comparing each one of the third plurality of read bits with a corresponding one of the fourth plurality of read bits; and

comparing each one of the first plurality of read bits with a corresponding one of the fourth plurality of read bits.